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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/709,800	11/09/2000	Min-Cheng Kao	JCLA-6349	4354

			EXAMINER
7590	02/13/2004		O BRIEN, BARRY J

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ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	**Applicant(s)**
Office Action Summary	09/709,800	KAO ET AL.
	Examiner	**Art Unit**
	Barry J. O'Brien	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>30 December 2003</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All   b)☐ Some *   c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1-16 have been examined.

Papers Submitted

2.   It is hereby acknowledged that the following papers have been received and placed on

record in the file: Amendment A as received on 12/30/2003.

Specification

3.   The lengthy specification has not been checked to the extent necessary to determine the

presence of all possible minor errors. Applicant's cooperation is requested in correcting any

errors of which applicant may become aware in the specification.

4.   The applicant is requested to review the specification and update the status of all co-

pending applications made mention of, replacing attorney docket numbers with current U.S.

application or patent numbers when appropriate.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

6.   Claims 1-4, and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seal

et al., U.S. Patent No. 5,583,804.

7.   Regarding claims 1 and 9, taking claim 1 as exemplary, Seal has taught an apparatus for

processing data (102 of Fig.1), said apparatus comprising:

         a.   A general register bank of N-bit data processing registers (106 of Fig.1);

         b.   A multiplier (108 of Fig.1 and 14,16,18,20 of Fig.6B) for performing multiply

                     operations upon a first operand and a second operand and outputting a 2N-bit

                     multiplied result (see Col.2 lines 58-65 and Col.17 lines 39-40);

         c.   An accumulator (108 of Fig.1), coupled to the multiplier and the general register

                     bank (see Fig.1), for performing accumulate operations upon the 2N-bit

                     multiplied result and the 2N-bit addition operand and outputting a 2N-bit

                     accumulated result (see Col.2 lines 3-8).

8.   Seal has not explicitly taught a special bank of N-bit data processing registers, the

selector coupled to the special register bank and the general register bank, for selecting one of

the special and general register banks and outputting a selected N-bit result from the selected

register bank, wherein the selected N-bit result and a N-bit data form a 2N-bit addition operand,

as well as having not taught the accumulator coupled to the selector.

9.   However, Seal has taught the general register bank (106 of Fig.1) having only two read

ports and taking at least two cycles for a multiply-accumulate instruction to execute (see Col.5

lines 60-64). It is well known in the art that reducing the amount of cycles that instructions take

to execute is of paramount concern. One of ordinary skill in the art at the time of the invention

would have recognized that placing two register banks with two read ports each allows 4 read

ports to be active at once. Therefore, it would have been obvious to one of ordinary skill in the

art to combine two general register banks in parallel in order to read out twice as many operands

in half as much time, reducing the amount of cycles a multiply-accumulate instruction takes to execute.

10.   Furthermore, one of ordinary skill in the art would have recognized the requirement for a selector, such as a multiplexer, to be connected between the two general register banks and the accumulator, to mediate and recognize the data coming out of the banks so that data from the correct locations gets processed instead of being arbitrarily put on a data bus without identification. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to place a selector connected to the outputs of the two general register banks in order to choose the correct data from the correct locations after it has been read from the banks.

11.   Claim 9 is nearly identical to claim 1, differing only in minor informalities in their claim language. Thus, claim 9 is rejected for the same reasons as claim 1.

12.   Regarding claims 2 and 10, taking claim 2 as exemplary, Seal has taught the apparatus for processing data of claim 1, wherein the N-bit data is held in the general register bank (see Col.3 lines 59-60 and Col.4 lines 1-2). The third and fourth data processing registers are located within the general register bank (106 of Fig.1) (see Col.3 lines 48-55).

13.   Claim 10 is nearly identical to claim 2, differing only in their parent claims, which are both rejected above. Thus, claim 10 is rejected for the same reasons as claim 2.

14.   Regarding claims 3 and 11, taking claim 3 as exemplary, Seal has taught the apparatus for processing data of claim 1, wherein the selector selects one of the special and general register banks. Seal has not taught the selector receiving a class signal and then selecting one of the register banks in response to the signal.

15.   However, Seal has taught a class signal which is used for indicating a first or second class

of instruction (see 36 of Fig.2 and Fig.3, also Col.5 lines 13-15 and 44-47). Because the first and

second classes of instructions require different numbers and combinations of operands to be read

from the register banks (see Col.3 lines 56-67 and Col.4 lines 1-7), one of ordinary skill in the art

would have recognized that class signal should be used in selecting the register bank from which

the operands are coming. Therefore, it would have been obvious to one of ordinary skill in the

art to control the selector between the register banks with a class signal so that the correct

register bank and operands could be selected based upon the class of an instruction being

executed.

16.   Claim 11 is nearly identical to claim 3, differing only in their parent claims, which are

both rejected above. Thus, claim 11 is rejected for the same reasons as claim 3.

17.   Regarding claims 4 and 12, taking claim 4 as exemplary, Seal has taught the apparatus

for processing data of claim 3, the class signal is used for indicating a first class of instruction or

a second class of instruction (see 36 of Fig.2 and Fig.3, also Col.5 lines 13-15 and 44-47),

wherein the first class of instruction is executing a first calculation of $N*N+2N\rightarrow2N$ and the

second class of instruction is executing a second calculation of $N*N+N\rightarrow N$ (see Col.2 lines 18-

22).

18.   Claim 12 is nearly identical to claim 4, differing only in their parent claims, which are

both rejected above. Thus, claim 12 is rejected for the same reasons as claim 4.

19.   Claims 5-8 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Seal et al, U.S. Patent No. 5,583,804 as applied to claims 1, 4-5 and 8 above, and further in view

of Morrison et al, U.S. Patent No. 6,581,086.

20.   Regarding claim 5, Seal has taught the apparatus for processing data of claim 4, but has

not taught the apparatus further comprising a detecting device, coupled to the accumulator, for

receiving the 2N-bit accumulated result and for checking if a case of overflow occurs.

21.   However, Morrison has taught a scaler (60 of Fig.9) connected to the accumulator (see

Fig.9) that contains a comparator that determines whether the result has overflowed (see Col.9

lines 24-42). One of ordinary skill in the art would have recognized that overflow detection is

desirable in order to prevent errors from propagating through a data processing system without

having to recalculate operations already performed (see Col.10 lines 54-58). Therefore, one of

ordinary skill in the art at the time of invention would have found it obvious to include a

comparator connected to the accumulator to detect overflow to prevent error propagation.

22.   Claim 13 is nearly identical to claim 5, differing only in their parent claims, which are

both rejected above, and in claim 13's lack of a detecting device. Thus, claim 13 is rejected for

the same reasons as claim 5.

23.   Regarding claims 6 and 14, taking claim 6 as exemplary, Seal has taught the apparatus

for processing data of claim 5, wherein:

> a.   The outputted N-bit result from the selector and the N-bit data held in the general
>
> register bank are formed in combination as a first N-bit part and a second N-bit part of
>
> the 2N-bit addition operand (see Col.3 lines 65-67 and Col.4 lines 1-7). It has already
>
> been shown above that N-bit data is held in the general register bank, and that a selector
>
> controlled by a class signal chooses the N-bit result from one of the two register banks.
>
> b.   The accumulated result includes a third N-bit part and a fourth N-bit part (see
>
> Col.4 lines 2-4);

24.   Seal has not taught that when the class signal is the second class of instruction, the
detecting device compares the first N-bit part of the 2N-bit addition operand and the third N-bit
part of the accumulated result to determine if the case of overflow occurs.

25.   However, Morrison has taught a scaler (60 of Fig.9) which contains a comparator (see
Col.9 lines 24-25). The comparator compares a portion of the expected value with the final
accumulated result (see Col.9 lines 1-9) and checks for equality. It is well known in the art that
here are various ways to check for overflow, such as sign checking or comparing portions of the
operands for equality or inequality, and these methods depend on the precision of the calculation
being checked. Because the accumulator which holds the final result is larger than an individual
operand (see Col.7 lines 61-63), one of ordinary skill in the art at the time of invention would
have recognized that when checking a portion of an accumulated result for equality with the
expected result, one only needs to check the most-significant bits which are larger than the
operand. Also, if the expected result is also the same size as an operand, then the portion of an
intermediate result, existing prior to the final addition, that is larger than an operand should
remain the same through the final calculation, and thus can be compared to the final result for
equality instead of calculating an expected result. Therefore, one of ordinary skill in the art
would have found it obvious to compare a first portion of the accumulated result to a first portion
of an intermediate result for equality when checking for overflow of an operation.

26.   Claim 14 is nearly identical to claim 6, differing only in their parent claims, which are
both rejected above, and in claim 14's lack of a detecting device. Thus, claim 14 is rejected for
the same reasons as claim 6.

27.   Regarding claim 7, Seal has taught the apparatus for processing data of claim 1, but has

not taught the apparatus further comprising a detecting device, coupled to the accumulator, for

receiving the 2N-bit accumulated result and for checking if a case of overflow occurs.

28.   However, Morrison has taught a scalar (60 of Fig.9) connected to the accumulator (see

Fig.9) that contains a comparator that determines whether the result has overflowed (see Col.9

lines 24-42). One of ordinary skill in the art would have recognized that overflow detection is

desirable in order to prevent errors from propagating through a data processing system without

having to recalculate operations already performed (see Col.10 lines 54-58). Therefore, one of

ordinary skill in the art at the time of invention would have found it obvious to include a

comparator connected to the accumulator to detect overflow to prevent error propagation.

29.   Claim 15 is nearly identical to claim 7, differing only in their parent claims, which are

both rejected above, and in claim 15's lack of a detecting device. Thus, claim 15 is rejected for

the same reasons as claim 7.

30.   Regarding claims 8 and 16, taking claim 8 as exemplary, Seal has taught the apparatus

for processing data of claim 7, wherein:

> a.   The outputted N-bit result from the selector and the N-bit data held in the general
>
> register bank are formed in combination as a first N-bit part and a second N-bit part of
>
> the 2N-bit addition operand (see Col.3 lines 65-67 and Col.4 lines 1-7). It has already
>
> been shown above that N-bit data is held in the general register bank, and that a selector
>
> controlled by a class signal chooses the N-bit result from one of the two register banks.
>
> b.   The accumulated result includes a third N-bit part and a fourth N-bit part (see
>
> Col.4 lines 2-4);

31.   Seal has not taught that when the class signal is the second class of instruction, the

detecting device compares the first N-bit part of the 2N-bit addition operand and the third N-bit

part of the accumulated result to determine if the case of overflow occurs.

32.   However, Morrison has taught a scaler (60 of Fig.9) which contains a comparator (see

Col.9 lines 24-25). The comparator compares a portion of the expected value with the final

accumulated result (see Col.9 lines 1-9) and checks for equality. It is well known in the art that

here are various ways to check for overflow, such as sign checking or comparing portions of the

operands for equality or inequality, and these methods depend on the precision of the calculation

being checked. Because the accumulator which holds the final result is larger than an individual

operand (see Col.7 lines 61-63), one of ordinary skill in the art at the time of invention would

have recognized that when checking a portion of an accumulated result for equality with the

expected result, one only needs to check the most-significant bits which are larger than the

operand. Also, if the expected result is also the same size as an operand, then the portion of an

intermediate result, existing prior to the final addition, that is larger than an operand should

remain the same through the final calculation, and thus can be compared to the final result for

equality instead of calculating an expected result. Therefore, one of ordinary skill in the art

would have found it obvious to compare a first portion of the accumulated result to a first portion

of an intermediate result for equality when checking for overflow of an operation.

Claim 16 is nearly identical to claim 8, differing only in their parent claims, which are both

rejected above, and in claim 16's lack of a detecting device. Thus, claim 16 is rejected for the

same reasons as claim 8.

Response to Arguments

33.   Applicant's arguments filed on 12/30/2003 have been fully considered but they are not

persuasive.

34.   On page 12, Applicant argues in regards to claims 1 and 9 in essence:

> *"Seal failed to disclose, teach or suggest, either implicitly or explicitly, the "special*
>
> *register bank of N-bit data processing registers" and the "selector" as claimed in claim*
>
> *1, and "selecting one of the special and general register banks and outputting a N-bit*
>
> *result from the selected register bank, wherein the N-bit result and a N-bit data form a*
>
> *2N-bit addition operand" as claimed in claim 9. Thus, the apparatus and method for*
>
> *processing data as claimed in claims 1 and 9 are totally different from that of Seal."*

35.   In response to applicant's argument that the references fail to show certain features of

applicant's invention, it is noted that the features upon which applicant relies (i.e., class signal

causing the selector to provide 2N bits of the of the addition signal including parts C and D,

which when the instruction is a first class, both are from the general register bank, and when of a

second class, C is from a special register bank and D is from the general register bank) are not

recited in the rejected claim(s) 1 and 9. The claim language simply states, *"A selector... for*

selecting one of the special and general register banks and outputting a selected N-bit result

from the selected register bank, wherein the selected N-bit result and a N-bit data form a 2N-bit

addition operand" in claim 1, and *"selecting one of the special and general register banks and*

outputting a N-bi result from the selected register bank, wherein the N-bit result and a N-bit data

form a 2N-bit addition operand" in claim 9, which are much more broad limitations than the

Applicant is arguing above. Furthermore, the Applicant admits that the features that they are

relying upon are located and defined within the specification (see p.12 line 1 of Amendment filed

on 12/30/2003). Although the claims are interpreted in light of the specification, limitations

from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26

USPQ2d 1057 (Fed. Cir. 1993), as well as the below citations.

36.   Applicant is arguing a feature of the invention not specifically stated in the claim
language, which is improper. Claimed subject matter, **not** the specification, is the measure of
invention. Limitations in the specification **cannot** be read into the claims for the purpose of
avoiding the prior art. *In re Self*, 213 USPQ 1,5 (CCPA 1982); *In re Priest*, 199 USPQ 11,15
(CCPA 1978).

"It is the claims that measure the invention." *SRI Int'l v. Matshshita Elec. Corp.*, 775 F.2d
1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc).

"The invention disclosed in Hiniker's written description may be outstanding in its field, but
the name of the game is the claim." *In re Hiniker Co.*, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

"[A]s an initial matter, the PTO applies to the verbiage of the proposed claims the broadest
reasonable meaning of the words in their ordinary usage as they would be understood by one of
ordinary skill in the art, taking into account whatever enlightenment by way of definitions or
otherwise that may be afforded by the written description contained in the applicant's
specification." *In re Morris*, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).

"Limitations appearing in the specification will not be read into the claims, and ... interpreting
what is meant by a word in a claim 'is not to be **confused with adding an extraneous limitation**
appearing in the specification, which is improper'." *Intervet Am., v. Kee-Vet Labs.*, 12 USPQ2d
1474, 1476 (Fed. Cir. 1989)(citation omitted).

"It is entirely proper to use the specification to interpret what the patentee meant by a word or
phrase in the claim, ... this is **not** to be confused with adding an extraneous limitation appearing
in the specification, which is improper. By 'extraneous,' we mean a limitation read into a claim
from the specification wholly apart from any need to interpret ... particular words or phrases in
the claim." *In re Paulsen*, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (citation omitted).

37.   Furthermore, the Applicant's arguments fail to comply with 37 CFR 1.111(b) because

they amount to a general allegation that the claims define a patentable invention without

specifically pointing out how the language of the claims patentably distinguishes them from the

references. The Examiner acknowledges that the examiner disagrees with his assertion that the

prior art of record, namely the Seal reference, teaches the limitations of claims 1 and 9.

However, the arguments which the Applicant relies upon, namely those in the first paragraph of

page 12, seem to be unrelated to prior art limitations summarized on page 11, and result in an

unwarranted conclusion in the second paragraph of page 12, as no differences between the prior

art of record and the invention have been established; i.e. **the Applicant has not pointed out**

how the Seal reference does not teach the limitations cited in the second paragraph of page

12.

38.   Although the argument presented on page 12 fails to show the differences between the

prior art of record and the claimed invention, as shown above, the Examiner, to the best of his

ability, believes he understands that the Applicant is arguing that the architectural organization of

the Applicant's invention is patentable over the Seal reference, specifically how and what

registers are selected for the two levels of precision in instructions. However, the Examiner

disagrees with the Applicant's argument. The rejection of claims 1 and 9 (see paragraphs 7-11

above) relies upon the duplication of the register file of Seal to get the effect of multiple register

files, specifically the increased number of registers and read ports (see In re Harza, 274 F.2d 669,

671, 124 USPQ 378, 380 (CCPA 1960))). Doing so, gives us two separate register files, one of

which we can consider to be "special", the other "general", and will effectively double the

number of registers addressable. Further, because Seal has taught a single register file being able

to read out two operands at a time (see Seal Col.5 lines 60-64), it follows that two register files

connected in parallel will be able to read out four operands at a time. Regarding the claimed

"selector", the claim language doesn't limit when the selector is to select between register files

for operands. Therefore, the selection in the rejection takes place at design time, instead of the

argued but unclaimed run-time, so that the high-precision instructions select and read from four

registers in parallel to get the operands (see Seal Fig.3), while the low-precision instructions

select and read from three registers in parallel to get the operands (see Seal Fig.2), wherein the

registers could be in either of the register files as necessitated by the two types of instructions.

Therefore, as set forth in paragraphs 7-11 above and further explained here, Seal has taught a

special register bank of N-bit data processing registers along with a selector as in claim 1, as well

as selecting one of the special and general register banks and outputting a N-bit result from the

selected register bank, wherein the N-bit result and a N-bit data form a 2N-bit addition operand

as in claim 9.

39.   On page 13, Applicant argues in regards to claims 1 and 9 in essence:

"Actually, the combination of Seal and the alleged well-known art still failed to disclose,

teach, or suggest either implicitly or explicitly, the "special register bank of N-bit data

processing register" and the "selector" as claimed in claim 1, and "selecting one of the

special and general register banks and outputting a N-bit result from the selected register

bank, wherein the N-bit result and a N-bit data form a 2N-bit addition operand", as

claimed in claim 9."

40.   Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a

general allegation that the claims define a patentable invention without specifically pointing out

how the language of the claims patentably distinguishes them from the references. The

Examiner acknowledges that the examiner disagrees with his assertion that the prior art of

record, namely the Seal reference in combination with well-known art, teaches the limitations of

claims 1 and 9. However, the arguments which the Applicant relies upon, namely those in the

third paragraph of page 13, seem to be unrelated to prior art summarized in paragraph 2 on page

13, and result in an unwarranted conclusion in the third paragraph of page 13, as no differences

between the prior art of record and the invention have been established; i.e. **the Applicant has**

not pointed out how the Seal reference does not teach the limitations cited in the third

paragraph of page 13.

41.   A further unsupported argument is made in this section also, albeit a secondary argument,

regarding claims dependent upon the argued claims 1 and 9 in the second paragraph of page 14.

This argument simply states, "... *The dependent claims recite further features and/or*

combinations of features that are patentably distinct from the prior art of record. For example,

dependent claim 3 further recites, "The selector further receiving a class signal, wherein the

selector selects one of the special and general register banks in response to the class signal," but

gives absolutely no justification for this conclusion, similar to the above argument.

42.   Although the argument presented on page 13 fails to show the differences between the

prior art of record and the claimed invention, as shown above, the Examiner, to the best of his

ability, believes he understands that the Applicant is arguing that the duplication of the register

file will only be able to output two instructions per cycle. The Examiner agrees with the

Applicant's assertion, but is unsure how it relates to the claimed invention, as no claims are

directed towards the amount of cycles that the invention takes to execute the multiply-

accumulate instructions. The rejection of claims 1 and 9 (see paragraphs 7-11 above) relies upon

the duplication of the register file of Seal to get the effect of multiple register files, specifically

the increased number of registers and read ports (see In re Harza, 274 F.2d 669, 671, 124 USPQ

378, 380 (CCPA 1960))). Because Seal has taught that one register file has two read ports,

reading one register per cycle, it directly follows that by duplicating the register file, one would

have the ability to have four read ports, reading two registers per cycle (one per register file).

Therefore, the amount of cycles needed to read the four registers necessary for a high-precision

multiply-accumulate instruction would be lowered to two cycles, an improvement over the

previous four cycles required with the single register file (see paragraph 9 above).

43.   On pages 15 and 16, Applicant argues in regards to claims 5 and 13 in essence:

"The overflow condition disclosed in the Morrison is the location of the first bit value

change with the location of the selected bits, which is totally different from the overflow

detection as claimed in the invention."

44.   In response to applicant's argument that the references fail to show certain features of

applicant's invention, it is noted that the features upon which applicant relies (i.e., comparing the

first N-bit part of the accumulated result with the first N-bit part of the addition operand to

determine overflow) are not recited in the rejected claim(s) 5 and 13. The claim language simply

states, *"A detecting device ... for receiving the 2N-bit accumulated result and for checking if a*

case of overflow occurs" in claims 5 and 13, which provides no indication as to how overflow is

being detected, just simply that it is being detected. Because no specific method for detecting

overflow is claimed, than prior art that teaches **any** method of overflow detection will read on

the claims, which the combination of Seal in view of Morrison does as shown above in

paragraph 21. Furthermore, the Applicant admits that the features that they are relying upon are

located and defined within the specification (see p.16 line 5 of Amendment filed on 12/30/2003).

Although the claims are interpreted in light of the specification, limitations from the specification

are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir.

1993), as well as the below citations.

45.   Applicant is arguing a feature of the invention not specifically stated in the claim
language, which is improper. Claimed subject matter, **not** the specification, is the measure of
invention. Limitations in the specification **cannot** be read into the claims for the purpose of
avoiding the prior art. *In re Self*, 213 USPQ 1,5 (CCPA 1982); *In re Priest*, 199 USPQ 11,15
(CCPA 1978).

"It is the claims that measure the invention." *SRI Int'l v. Matshshita Elec. Corp.*, 775 F.2d
1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc).

"The invention disclosed in Hiniker's written description may be outstanding in its field, but
the name of the game is the claim." *In re Hiniker Co.*, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

"[A]s an initial matter, the PTO applies to the verbiage of the proposed claims the broadest
reasonable meaning of the words in their ordinary usage as they would be understood by one of
ordinary skill in the art, taking into account whatever enlightenment by way of definitions or
otherwise that may be afforded by the written description contained in the applicant's
specification." *In re Morris*, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).

"Limitations appearing in the specification will not be read into the claims, and ... interpreting
what is meant by a word in a claim 'is not to be **confused with adding an extraneous limitation**
appearing in the specification, which is improper'." *Intervet Am., v. Kee-Vet Labs.*, 12 USPQ2d
1474, 1476 (Fed. Cir. 1989)(citation omitted).

"It is entirely proper to use the specification to interpret what the patentee meant by a word or
phrase in the claim, ... this is **not** to be confused with adding an extraneous limitation appearing
in the specification, which is improper. By 'extraneous,' we mean a limitation read into a claim
from the specification wholly apart from any need to interpret ... particular words or phrases in
the claim." *In re Paulsen*, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (citation omitted).
46.

Conclusion

47.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing

date of this final action.

48.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864.

The examiner can normally be reached on Mon.-Fri. 7:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

49.   Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
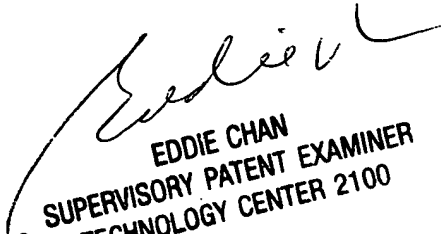
Barry J. O'Brien
Examiner
Art Unit 2183

BJO
2/10/04

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100